John T. Anderson

Engineering Note

Date: May 3rd, 2004
Rev Date: May 12th, 2004

Project: AFE II
Doc. No: A1040503

Subject: Summary List of Changes, AFE I to AFE II

Introduction

This summary document is provided as a convenience to the AFE II reviewers so that they may concentrate on things changed from the previous version.

General Change List

1. The SIFT/SVX Multi-Chip-Modules (MCMs) of the AFE I have been removed, to be replaced by two TRIP chips and two A/D converters each.
    - 1.1. As a result of (1), the octal DACs used to develop the threshold and VREF voltages for the SIFTs are removed.
        - 1.1.1. As a result of (1.1), the analog multiplexer used to create multiple I_2C sub-buses for the microprocessor has been removed.
    - 1.2. As a result of (1), the linear regulators for the SIFT/SVX have been replaced with different linear regulators with different output voltages.
        - 1.2.1. Since the TRIP & A/D chips only require +2.5V, the source +5.5V used for the SIFT/SVX regulators can be moved downwards to +3.3V while still maintaining regulation headroom. This removes some power dissipation from the board but necessitates changing the modules used in the bulk DC power supply.
    - 1.3. Because the TRIP chip is not compatible with +3.3V logic swings, additional buffer/level translator chips have been added to interface between the +3.3V digital logic and the TRIP.
    - 1.4. Separate linear regulators have been provided for the A/D converters and the two TRIP chips.
2. Xilinx FPGAs have been put down in place of the VSVX_MUX CPLDs used in the previous design, to provide a larger amount of logic capability and to provide FIFO buffering for the output of the ADCs of (1) above.
    - 2.1. These same FIFOs have also subsumed the responsibilities of the Event Delay FIFOs and Collector FIFO of the extant design, and thus these parts have been removed.
    - 2.2. The FPGAs require +3.3V for I/O compatibility with the rest of the board but require +2.5V for the core voltage.
        - 2.2.1. A high-side MOSFET switch and a separate linear regulator have been provided to generate the local +2.5V.
            - 2.2.1.1. In order to control and monitor these new parts, one new 8-bit output latch and one new dual 8-bit input buffer have been added to the microprocessor's data bus.
        - 2.2.2. The separate MOSFET switch part is required to allow the on-board microprocessor to sequence the turn-on of the FPGAs so as to not blow fuses from initial inrush current.
            - 2.2.2.1. Since the FPGA is expected, after settling from the inrush, to consume at least equal and probably larger power than the CPLD it replaced, the total +3.3V system power has now

exceeded that available from the bulk supply. Removal of the discrete FIFOs has provided a compensatory drop in the +5V supply that assuages total power dissipation concerns.

2.2.2.2. Separate linear regulators for three other CPLDs have been put into the board so that their power dissipation is moved from the +3.3V digital supply to the +5V digital supply, to keep the +3.3V total current within the limits of the bulk supply's capabilities.

2.2.3. Use of an FPGA rather than a CPLD means that the logic is now voltatile and external non-volatile storage for the code is required. A Flash Ram has been added to the board for this purpose.

2.2.3.1. The amount of microcontroller code required to support the Flash Ram exceeds the amount of spare space in the current microcontroller. Thus, the extant microcontroller has been replaced by one with twice the code space.

2.2.3.1.1. The new microcontroller doesn't have as good an A/D converter as the old one did, so an external A/D converter for handling the cyrostat monitoring functions has been added.

2.2.3.1.2. The address bus originally used for ram access isn't big enough to handle the Flash, so an external holding register for the additional address bits has been added to the microprocessor's data bus.

2.3. The readout architecture and timing is changed by removal of the Collector FIFO and so the design of the VSVX CPLD has to be changed. One of these changes is that the VSVX must now control the DVALID signal to the Sequencer. This requires adding a tapped delay line connected to the VSVX to obtain fine control over the clock phasing to insure that the VSVX can generate DVALID at the appropriate time relative to the assertion of data by the FPGAs when they are read out.

2.3.1. In the same regard the buffers between the AFE and the Sequencer have been rewired so that the VSVX can, if necessary, re-latch the data from the FPGAs prior to asserting it onto the cable running to the Sequencer.

2.3.2. The combination of the above will allow the VSVX to explicitly control the setup & hold time of TRIP ADC data to the Sequencer relative to the DVALID signal.

3. A known problem in the AFE I is that the analog multiplexers used in the cryostat controls can, under certain conditions, latch up. A power cycle is required to recover.

3.1. The analog multiplexers have been replaced with different multiplexers that will not latch up because they have wider power supply rails.

3.1.1. The new multiplexers require some external control and so an I2C control latch has been added.

3.1.2. To assuage concerns about the latchup condition propagating into the new ADC, a protection resistor and filter cap has been added between the muxes and the ADC.

4. Another known issue in the AFE I is frailties in the power monitoring circuit. A new power monitor chip has replaced the old one.

4.1. In addition the new microcontroller's ADC – while not sufficient for cryo monitoring – is sufficient for local voltage monitoring. Connections have been put in to allow for this.

5. In response to user requests, the VSVX CPLD is now connected to the geographic address pins to allow the geographical address of the board to be put into the readout stream.

6. In response to user requests, additional signal lines and a bi-directional register have been added between the microcontroller and the dual-port ram to insure no possible address contention between microcontroller and external MIL-STD 1553 accesses. A state machine in the 1553 controller CPLD is added to timeslice access to the DPRAM such that contentions are resolved in cycles shorter than either bus can access the memory.